Positive-Bias Temperature Instability (PBTI) of GaN MOSFETs

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***Abstract* — We have investigated the stability of the gate stack of GaN n-MOSFETs under positive gate stress. Devices with a gate dielectric that consists of pure SiO_2 or a composite SiO_2/Al_2O_3 bilayer were studied. Our research has targeted the evolution of threshold voltage (V_T), subthreshold swing (S) and transconductance (g_m) after positive gate voltage stress of different duration at different voltages and temperatures. We have also examined the recovery process after the stress is removed. We have observed positive V_T shift (ΔV_T) in both gate dielectrics under positive gate stress. In devices with a SiO_2 gate oxide, we have found that ΔV_T is caused by a combination of electron trapping in pre-existing oxide traps and interface trap generation. In devices with a composite SiO_2/Al_2O_3 gate oxide, on the other hand, ΔV_T is due to electron trapping in pre-existing oxide traps and generation of near interface oxide traps.**

Keywords-component; GaN; MOSFETs; BTI; V_T shift

I. INTRODUCTION

GaN power transistors represent a promising alternative to Si devices for power switching applications [1]. Compared to other semiconductor systems, GaN-based materials offer superior characteristics and performance under high-frequency and high-temperature conditions [2-4]. Recently, GaN-high electron mobility transistors with insulated-gate (MIS-HEMTs) have attracted much attention because they offer high current, high breakdown voltage and low gate leakage current, all desirable attributes for power transistors [5-7]. On the other hand, GaN MIS-HEMTs face significant reliability and stability challenges. Among them, instability of the electrical characteristics, in particular V_T, after prolonged high voltage stress at high temperature is a serious problem [8-11].

The problem of V_T instability is not unique to GaN transistors. This phenomenon has been intensively studied in Si, SiC and various III-V MOS systems where it is sometimes referred to as bias-temperature instability (BTI) [12-18]. In Si n-channel MOSFETs with high-k gate dielectric, Positive Bias Temperature Instability (PBTI) is known to be caused by electron trapping in pre-existing oxide traps that causes a positive V_T shift [12, 13]. Negative-bias temperature instability (NBTI) in p-channel MOSFETs is related to interface state generation and hole trapping in the gate dielectric [14]. In SiC MOSFETs, periodic V_T shifts under alternating positive and negative gate stress have been observed and attributed to electron tunneling in and out of near-interface oxide traps [15]. InGaAs n-MOSFETs with a high-k dielectric also have shown positive V_T shifts after positive gate stress. This is believed to be due to pre-existing oxide traps and electron trap generation near the oxide/InGaAs interface [16-18].

For GaN MIS-HEMTs, a few studies have reported V_T shifts due to PBTI [8-10]. However, its origin is not well understood. This is partly due to the complicated nature of the gate stack of a MIS-HEMT which contains several interfaces.

To better understand the mechanisms responsible for V_T shift under PBTI, a GaN MOSFET structure is desirable because of its single oxide/GaN interface. In [11], the V_T instability under PBTI in GaN MOSFETs with a SiN gate dielectric was studied. This work revealed the importance of the conduction band discontinuity at the oxide-semiconductor interface. However, the study did not include an evaluation of the changes in the subthreshold swing nor the transconductance of the device. These factors are important in themselves and greatly illuminate the relevant physics that affect the stability of V_T.

In this work, we examine the dynamics of V_T, S and g_m in GaN MOSFET before, during and after stress. This allows us to isolate and identify different mechanisms for V_T shift. We examine two different gate dielectrics: SiO_2 and a SiO_2/Al_2O_3 composite.

II. EXPERIMENTAL

A. Device structure

The devices studied in this work are sketched in Fig. 1 (not to scale). This is a simple recessed-gate structure with an intrinsic gate stack that consists of either 50 nm of SiO_2 or 40 nm EOT composite SiO_2/Al_2O_3 dielectric (Al_2O_3 next to semiconductor). The devices have channel width/length of 100 µm/1 µm. The standard figures of merit in the saturation regime (V_{DS} = 10 V) are for SiO_2 devices: V_T ~ -1.0 V, S ~ 175 mV/dec, g_{m_max} ~ 20 mS/mm; for SiO_2/Al_2O_3 devices: V_T ~ -0.7 V, S ~ 170 mV/dec, g_{m_max} ~ 30 mS/mm.

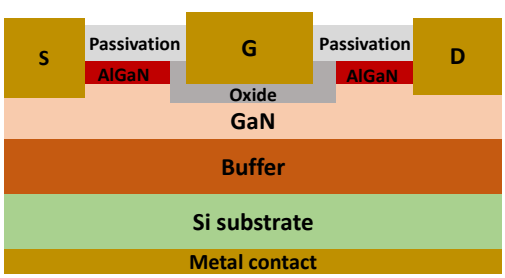

Figure 1. GaN MOSFET structure studied in this work.

In this study we focus our interest on the stability of the threshold voltage (V_T, defined at drain current I_D = 1 µA/mm), the subthreshold swing (S, defined at I_D = 0.1 µA/mm) and the maximum transconductance ($g_{m,max}$) in the linear region (defined at V_{DS} = 0.1 V). Virgin devices used in this work exhibit values of V_T = 0.06 V with a standard deviation of 0.096 V, S = 110 mV/dec, $g_{m,max}$ = 0.65 mS/mm for SiO_2 MOSFETs and V_T = 0.16 V with a standard deviation of 0.06 V, S = 100 mV/dec, $g_{m,max}$ = 0.56 mS/mm for SiO_2/Al_2O_3 MOSFETs. Fig. 2 shows the subthreshold and transconductance characteristics at different temperatures of SiO_2 and SiO_2/Al_2O_3 transistors in the linear regime (V_{DS} = 0.1 V).

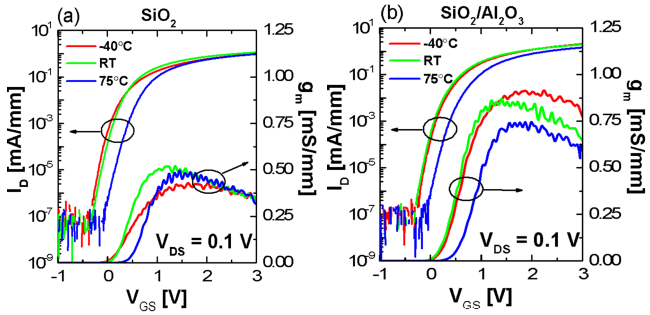

Figure 2. Subthreshold and transconductance characteristics of (a) SiO_2 and (b) SiO_2/Al_2O_3 GaN MOSFETs in the linear regime (V_{DS} = 0.1 V) at different temperatures.

B. *Experiment flow*

In our studies, we first developed a benign characterization scheme that is used to characterize the devices before, during and after stress experiments. It consists of an I_D-V_{GS} sweep at V_{DS} = 0.1 V that starts at V_{GS} = -0.5 V and stops at I_D = 1 µA/mm. From this we extract V_T and the subthreshold swing (S), as defined above. This method is benign as proven by minor changes in device characteristics after 100 sweeps (ΔV_T < 30 mV, ΔS < 20 mV/dec).

In a typical experiment, a device is first "initialized" and then characterized. The device initialization process consists of flushing the device for 5 minutes under microscope light, followed by thermal detrapping (we use a single set of thermal detrapping conditions throughout this work). Initialization typically results in a small change in device characteristics (ΔV_T < 30 mV). This step helps us create a "stable" and reproducible initial state for the device which we use as a reference for subsequent stress/recovery experiments. After initialization, we characterize the device with a complete I_D-V_{GS} sweep at V_{DS} = 0.1 V that starts at V_{GS} = -0.5 V and stops at V_{GS} = 3 V. From this sweep we extract the initial V_T, S and $g_{m,max}$. Next, the thermal detrapping step is repeated. We then re-measure the device with a shorter, benign I_D-V_{GS} sweep as described in the previous paragraph to confirm that the device characteristics are stable. At this point, the stress experiments can start.

The PBTI stress phase consists of a series of stress segments of increasing length, t_{stress}, during which the device is subject to a constant positive gate stress ($V_{GS,stress}$), with the source, drain and substrate grounded. $V_{GS,stress}$ between 5 and 15 V and t_{stress} between 10 and 10,000 seconds have been studied at -40°C, room temperature (RT) and 75°C. Immediately after each stress segment, the evolution of V_T and S are tracked through repeated I_D-V_{GS} sweeps that are performed for ~1,000 sec. The first reading comes 1 to 2 sec after the stress is stopped. At the end of each stress segment, the device is reinitialized using thermal detrapping and a complete characterization is performed. To confirm that the thermal detrapping is effective and complete, in several cases we have periodically remeasured a stressed and thermally detrapped device after storage at room temperature of various lengths of time. We have not observed any significant additional recovery of V_T within 10^7 s. We then consider the residual ΔV_T, ΔS and Δg_{m_max} after thermal detrapping permanent. In a typical sequence, the same device is used starting from the lowest $V_{GS,stress}$ and shortest t_{stress}. If permanent damage occurs after a stress step, i.e., V_T and S are not restored to their initial values after thermal detrapping, we switch to a new device with well-matched initial characteristics.

In a separate set of experiments, we use a fresh collection of devices to study the behavior of $g_{m,max}$. We perform similar stress and recovery experiments but immediately after each stress segment we perform a one-time, downward sweep of I_D-V_{GS} in the linear region (V_{DS} = 0.1 V) that starts at V_{GS} = 5 V and stops at V_{GS} = – 0.5 V. Because $V_{GS,stress}$ is at least 5 V, this sweep should not introduce additional damage to the device. Since the maximum transconductance point tends to occur between V_{GS}=2.5 and 4 V, this sweep yields a measurement of $g_{m,max}$ in the linear regime.

III. RESULTS

A. *Positive gate stress at room temperature (RT)*

Fig. 3 (a) shows the stress time evolution of ΔV_T under positive gate stress for SiO_2 and SiO_2/Al_2O_3 GaN MOSFETs at RT. Data points are extracted 1 sec after the stress is stopped. For both dielectrics, we observe positive ΔV_T that increases with t_{stress} and $V_{GS,stress}$. The composite dielectric generally shows more V_T shift than the pure SiO_2 gate. The evolution of ΔS is shown in Fig. 3 (b). For the SiO_2 devices, we see minimal change in S for $V_{GS,stress}$ = 5 and 10 V, but a clear increase for $V_{GS,stress}$ = 15 V. For the SiO_2/Al_2O_3 device, we see minimal change in S at all $V_{GS,stress}$.

Fig. 4 shows the dynamics of V_T and S recovery at RT after $V_{GS,stress}$ = 5 V and 15 V for t_{stress} = 10,000 s. We observe partial ΔV_T recovery and no ΔS recovery

Introducing a final detrapping step following the recovery phase allows us to assess the introduction of permanent damage during the stress phase. The open symbols in Figs. 3 and 4 show final values of ΔV_T and ΔS after 10,000 sec stress segments followed by thermal detrapping. The devices experience a nearly complete recovery after 5 V stress, but only partial recovery after 15 V stress. Notably, ΔS after 15 V stress did not recover at all in the SiO_2 MOSFETs. I_D-V_{GS} curves before stress and after stress and thermal detrapping for V_{GS_stress} = 15 V are shown in Fig. 5.

In general, in all studied devices, we find no significant permanent V_T shift after $V_{GS,stress} \leq$ 10 V, but a permanent component for $V_{GS,stress}$ = 15 V. For the SiO_2/Al_2O_3 devices,

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we observe no significant permanent S degradation. For SiO_2 devices, S degrades after 15 V stress and is not recoverable. This also suggests the introduction of permanent damage to these devices.

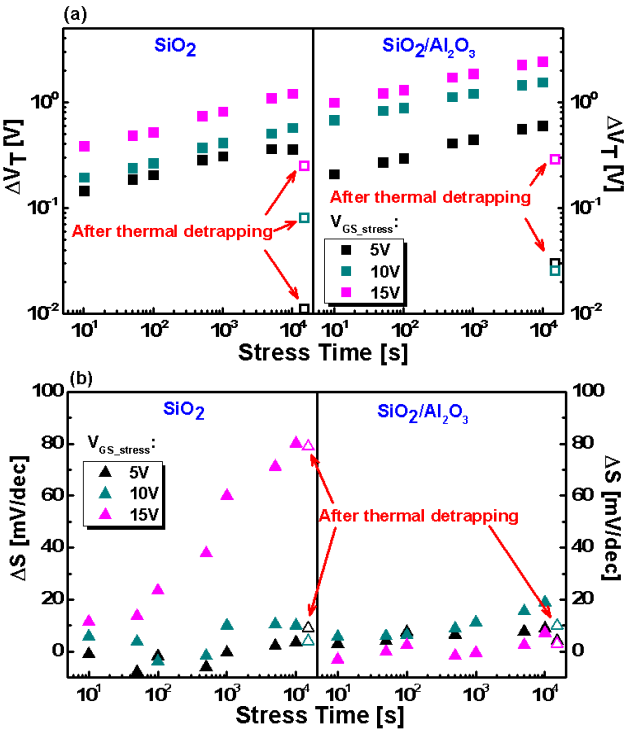

Figure 3. (a) Stress time evolution of ΔV_T, (b) stress time evolution of ΔS, for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs stressed at three different voltages at room temperature. Data points are taken 1 sec after the stress. The last set of points (open symbols) are ΔV_T and ΔS after thermal detrapping following a stress experiment with t_{stress} = 10,000 s.

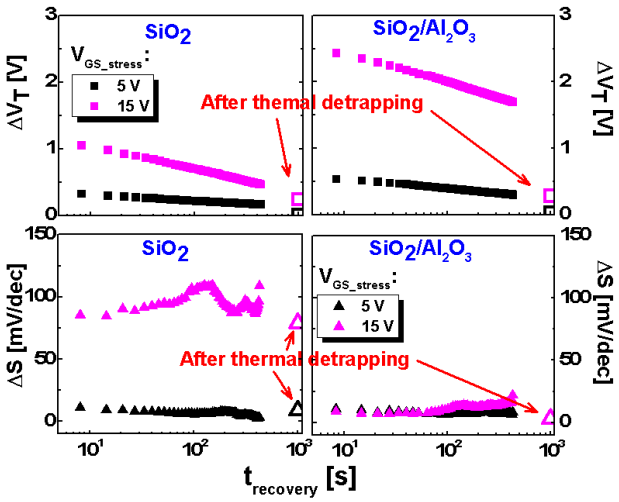

Figure 4. Recovery of ΔV_T and ΔS after a 10,000 sec stress at RT for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs at $V_{GS,stress}$ = 5 and 15 V. The last set of points (open symbols) are ΔV_T and ΔS after thermal detrapping following the recovery phase.

During each stress segment, we also monitor the evolution of the gate current (I_G). Fig. 6 shows I_G as a function of stress time for t_{stress} = 10,000 sec experiments. I_G tends to slightly decrease with stress time. This is consistent with other studies on charge trapping in pre-existing oxide traps. It also indicates that no new trap generation is occurring [19].

Fig. 7 shows the evolution of $g_{m,max}$ degradation ($\Delta g_{m,max}/g_{m,max0}$) ~ 1 sec after stress (closed symbols) and after subsequent thermal detrapping (open symbols) in a separate set of experiments from those of Figs. 2-6. For both dielectrics, we see higher $g_{m,max}$ degradation with higher $V_{GS,stress}$ and longer t_{stress}. At $V_{GS,stress}$ = 5 V, g_m degradation is minimal. After thermal detrapping, g_m completely recovers in SiO_2 MOSFETs, and only partially recovers in SiO_2/Al_2O_3 MOSFETs.

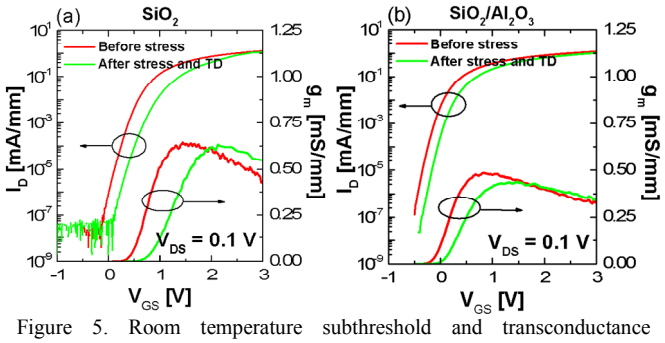

Figure 5. Room temperature subthreshold and transconductance characteristics before and after V_{GS_stress} = 15 V stress followed by thermal detrapping (TD) of (a) SiO_2 and (b) SiO_2/Al_2O_3 GaN MOSFETs in the linear regime (V_{DS} = 0.1 V).

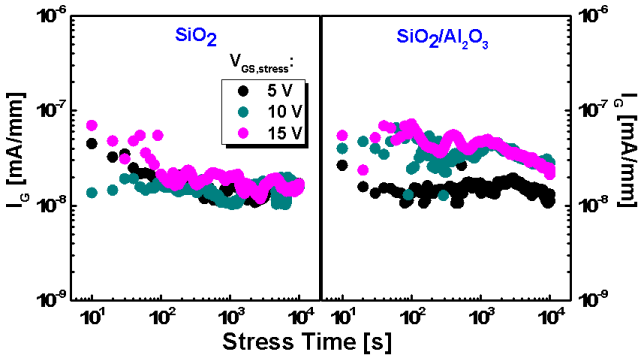

Figure 6. Stress time evolution of I_G for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs stressed at three different voltages at room temperature.

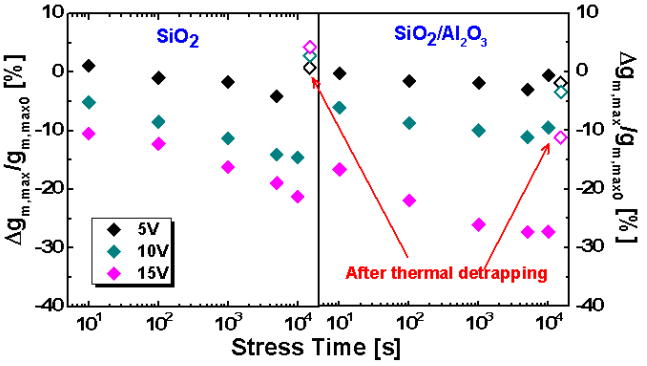

Figure 7. Stress time evolution of $\Delta g_{m,max}/g_{m,max0}$ for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs stressed at three different voltages at room temperature. Data points are taken ~1 sec after the stress is stopped. The last set of points (open symbols) are $\Delta g_{m,max}/g_{m,max0}$ after thermal detrapping following a t_{stress} = 10,000 s stress experiment.

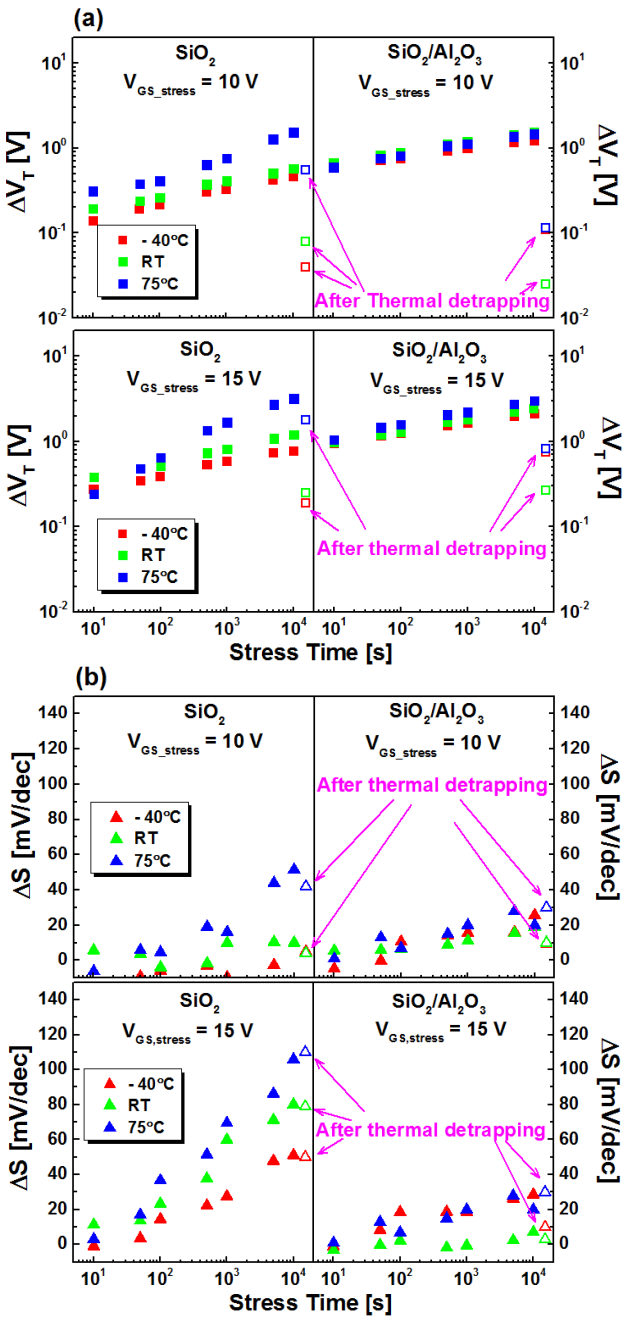

Figure 8. Stress time evolution of (a) ΔV_T and (b) ΔS for SiO_2 vs SiO_2/Al_2O_3 GaN MOSFETs at different T. $V_{GS,stress}$ = 10 and 15 V. Data points are taken 1 sec after the stress. The last set of points (open symbols) are ΔV_T and ΔS after a thermal detrapping step that follows stress experiments with t_{stress} = 10,000 s.

B. Impact of stress temperature

We have also studied the role of temperature during electrical stress. Fig. 8 shows ΔV_T and ΔS for $V_{GS,stress}$ = 10 and 15 V as a function of stress time at different temperatures. The stress and recovery phases take place at the same temperature. For SiO_2, ΔV_T and ΔS increase with T, and the increase is more prominent at 75°C. On the other hand, the effect of T is small for SiO_2/Al_2O_3 transistors at V_{GS_stress} = 10 V, while at V_{GS_stress} = 15 V, it becomes more prominent. However, this T dependence is less than in SiO_2 transistors.

The recovery dynamics of V_T and S after $V_{GS,stress}$ = 10 V and 15 V at different T are graphed in Fig. 9. The recovery time constants of both SiO_2 and SiO_2/Al_2O_3 devices appear rather independent of temperature. The final values of ΔV_T and ΔS after thermal detrapping for t_{stress} = 10,000 sec at various T are marked as open symbols (also summarized in Fig. 8 (open symbols)). Device characterization after thermal detrapping is made at the same temperature as the stress and recovery phases of the experiment.

For $V_{GS,stress}$ = 10 V, after thermal detrapping, ΔV_T mostly recovers for the SiO_2/Al_2O_3 transistors at all T. The SiO_2 transistors recover for T ≤ RT and only partially recover for T = 75°C. Also at T = 75°C, S exhibits some permanent damage for SiO_2 transistors. The SiO_2/Al_2O_3 transistors, on the other hand, exhibit minor permanent damage in S.

For $V_{GS,stress}$ = 15 V, after thermal detrapping, ΔV_T partially recovers for all transistors at all T. For the SiO_2 transistors,

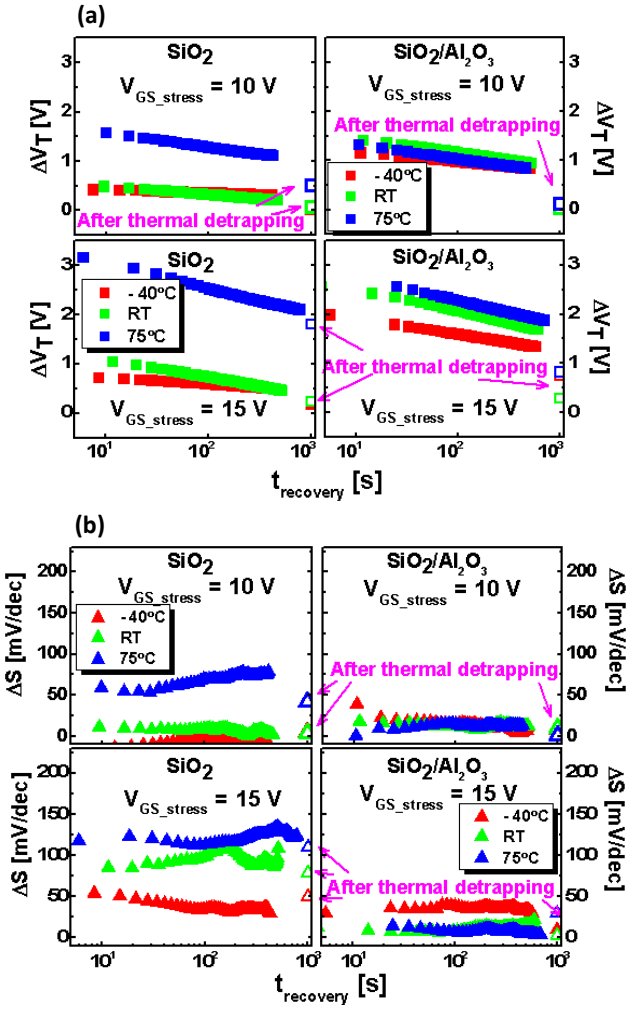

Figure 9. Recovery of (a) ΔV_T and (b) ΔS after a 10,000 sec stress at $V_{GS,stress}$ = 10 and 15 V for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs at -40°C, RT and 75°C. The last set of points (open symbols) are ΔV_T and ΔS after subsequent thermal detrapping step.

there is more recovery for T ≤ RT than for T = 75°C. Also for SiO_2 transistors, S exhibits permanent damage at all T, and the permanent damage increases with T. The SiO_2/Al_2O_3 transistors again exhibit small permanent S damage. Again, I_G during stress tends to slightly decrease with stress time (not shown here).

IV. Discussion

A. *Mechanisms responsible for V_T shift under PBTI*

Our experiments allow us to postulate the mechanisms responsible for PBTI in GaN MOSFETs. Under benign stress ($V_{GS,stress}$ ≤ 10 V, T ≤ RT), the V_T shift is consistent with electron trapping in pre-existing oxide traps which is characterized by a recoverable ΔV_T. We conclude this from Figs. 8(a) and 9(a) that show ΔV_T 1 sec after different stress times. Within such a short time, little recovery takes place (Fig. 9 shows long recovery time constant). Stress time evolution of V_T follows a saturating log-time dependence, as observed in other MOS systems [15-17,19]. The slight decrease in I_G also indicates that no additional traps are generated in the oxide bulk [19].

Under harsher stress ($V_{GS,stress}$ = 15 V), there is an additional permanent V_T shift for both gate dielectrics. Fig. 10 summarizes the final ΔV_T and ΔS after thermal detrapping for each stress segment at room temperature. Notably, SiO_2 exhibits a significant permanent increase in S that suggests the generation of interface states. This is clearer in Fig. 11 that graphs the correlation between the final values of ΔV_T and ΔS after thermal detrapping following electrical stress at $V_{GS,stress}$ = 15 V. We see a strong linear correlation between the two. The proportionality constant seems to depend on T. Subthreshold swing degradation under PBTI has also been reported in Al_2O_3/InGaAs and HfO_2/GaAs MOSFETs [18,20]. In our composite oxide samples, the permanent degradation of S is minor and a clear correlation with ΔV_T does not emerge.

An additional interesting observation in our work is that the evolution of $g_{m,max}$ and V_T also seem correlated. This can be seen in Fig. 12 that graphs $\Delta g_{m,max}/g_{m,max0}$ as a function of ΔV_T after different stress periods for both dielectrics at room temperature. With the exception of long t_{stress} in SiO_2/Al_2O_3 transistors, we observe a strong linear correlation between

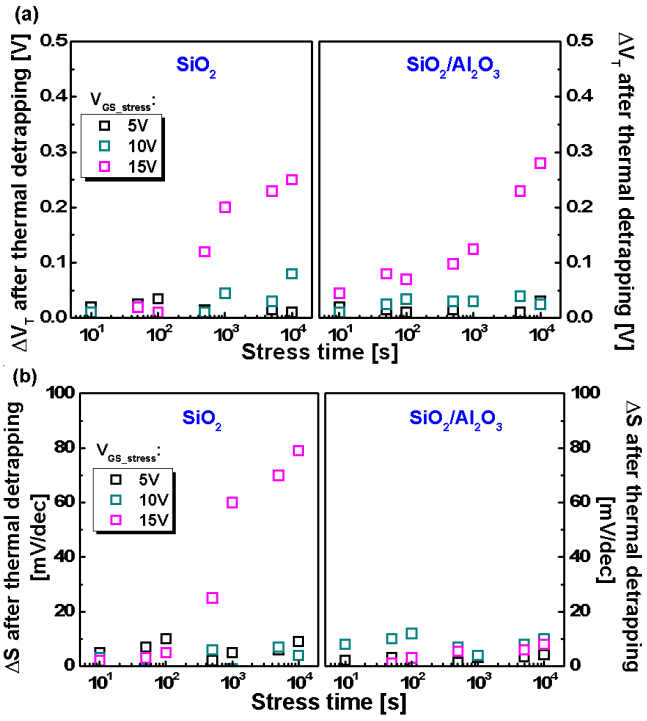

Figure 10. Final values of (a) ΔV_T and (b) ΔS after thermal detrapping vs. stress time for SiO_2 vs. SiO_2/Al_2O_3 GaN MOSFETs stressed at three different voltage at room temperature.

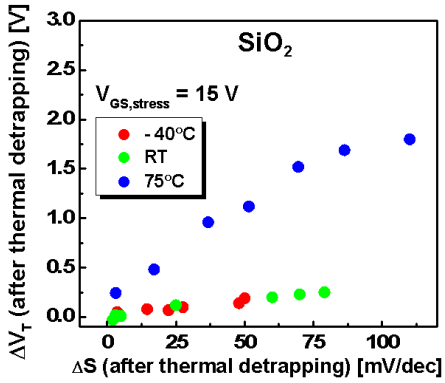

Figure 11. Evolution of final values of ΔV_T vs. ΔS for SiO_2 transistors after $V_{GS,stress}$ = 15 V at different temperatures. All measurements were taken at room temperature after a thermal detrapping step.

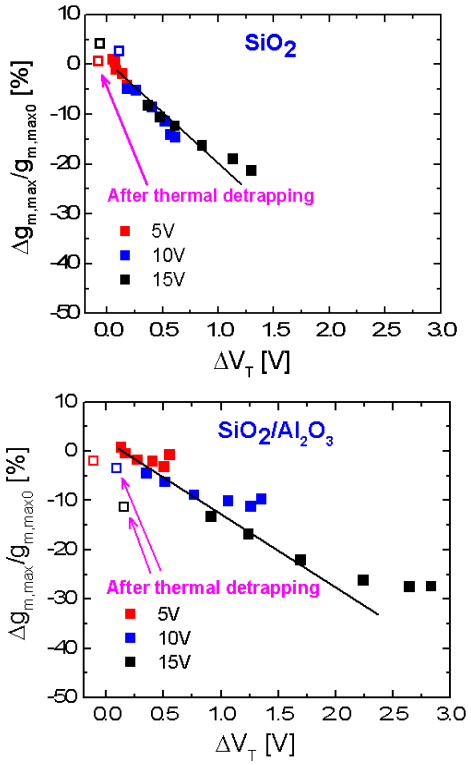

Figure 12. Evolution of ($\Delta g_{m,max}/g_{m,max0}$) vs. ΔV_T for (a) SiO_2 and (b) SiO_2/Al_2O_3 transistors during stress experiments of various durations at room temperature. The open symbols correspond to measurements after a thermal detrapping step following stress experiments with t_{stress} = 10,000 s.

$\Delta g_{m,max}/g_{m,max0}$ and ΔV_T at all $V_{GS,stress}$ for both dielectrics. This suggests that ΔV_T mostly originates in charge trapping in the oxide near the oxide/GaN interface or at the interface itself in interface states. Both are known to affect the mobility [17, 22]. For long stress times, trapping further away from the interface eventually takes place producing an additional V_T shift without a corresponding decrease in $g_{m,max}$.

$\Delta g_{m,max}/g_{m,max0}$ vs. ΔV_T after thermal detrapping following stress experiments with t_{stress}=10,000 s are also reported in Fig. 12 (open symbols). We see permanent degradation of $\Delta g_{m,max}/g_{m,max0}$ for the SiO_2/Al_2O_3 transistors after $V_{GS,stress}$ = 15 V, which suggests new trap generation in the oxide near the oxide/GaN interface that causes permanent mobility degradation [17, 23, 24]. Because these trap sites are far from the gate metal, no significant changes are observed in the evolution of I_G. This oxide trap generation close to the oxide/GaN interface also explains the incomplete recovery after thermal detrapping of V_T for the SiO_2/Al_2O_3 transistor after $V_{GS,stress}$ = 15 V that is apparent in Figs. 3(a), 8 and 12.

B. Model

The observations that we have made here are largely consistent with similar experiments on Si, SiC and III-V MOSFETs [15-18]. ΔV_T appears to take place due to two mechanisms. One component, ΔV_{Tox}, arises from electron trapping in the oxide. A second component, ΔV_{Tit}, which correlates to ΔS, originates in interface state generation and population.

We postulate that, to the first order, for SiO_2 MOSFETs, ΔV_{Tit} is the permanent portion of ΔV_T that is left after thermal detrapping. This hypothesis is supported by the linear dependence that we observe between the permanent portion of ΔV_T and of ΔS (Fig. 11) which strongly suggests the generation of interface states. Similar observation of interface state generation has been made in Si systems after radiation [25], and also in FinFETs [26] where the [110] Si surface has a much higher Si-H bond density compared to the [100] surface [27]. It is well known that hydrogen used to passivate dangling bonds at the oxide-semiconductor interface can escape leading to the creation of interface states [28]. The remainder of ΔV_T for the SiO_2 transistors is ΔV_{Tox}.

For SiO_2/Al_2O_3 MOSFETs, ΔV_{Tox} dominates and the permanent portion of ΔV_T is oxide trap generation close to the oxide/GaN interface, as observed in InGaAs n-MOSFETs [17]. The interface state generation in SiO_2/Al_2O_3 appears negligible, which is consistent with literature on high-K dielectrics [19].

With this interpretation, we find that ΔV_{Tox} in both transistor types follows a classic saturating log-time dependence, as observed in other MOS systems. The model of this power law relationship is described by [19]:

$$\Delta V_{Tox} = \Delta V_{max} \cdot \left\{1 - exp\left(-\left(\frac{t_{stress}}{\tau_0}\right)^{\beta}\right)\right\} \qquad (1)$$

where ΔV_{Tox} is the V_T shift due to oxide trapping. ΔV_{max} is a function of total trap density and the centroid of the trap-charge distribution in space, β describes the trap energy distribution, and τ_0 is the time constant of the traps. For the SiO_2/Al_2O_3 system, an exponent β = 0.22 ~ 0.25 and τ_0 = 200 s gives an excellent fit to the entire data set at all T (Fig. 13). For the SiO_2 system, β = 0.25 and τ_0 = 150 s provides a reasonable match at all T. The β values extracted here are close to those reported in the literature: β = 0.2 ~ 0.32 [15-18].

For $V_{GS,stress}$ = 15 V in SiO_2 MOSFETs, there is an additional component of ΔV_T that we attribute to interface state generation (ΔV_{Tit}) [25]. As we can see in Fig. 11, there is a linear dependence between ΔV_{Tit} and ΔS which is precisely what is expected from a simple model [25].

For SiO_2/Al_2O_3 MOSFETs, there is also a non-recoverable ΔV_T component for $V_{GS,stress}$ = 15 V. This permeant ΔV_T is accompanied by a non-recoverable $g_{m,max}$ degradation as shown in Fig. 7. This indicates permanent mobility degradation. Studies have attributed this to the generation of oxide traps close to the oxide/semiconductor interface [17,22].

V. CONCLUSIONS

In conclusion, we have studied PBTI of GaN MOSFETs with SiO_2 and SiO_2/Al_2O_3 as gate dielectric. For SiO_2 MOSFETs, a positive ΔV_T is caused by a combination of electron trapping in pre-existing oxide traps and interface trap generation. For SiO_2/Al_2O_3 MOSFETs, a positive V_T shift is due to trapping in the pre-existing oxide traps and oxide trap

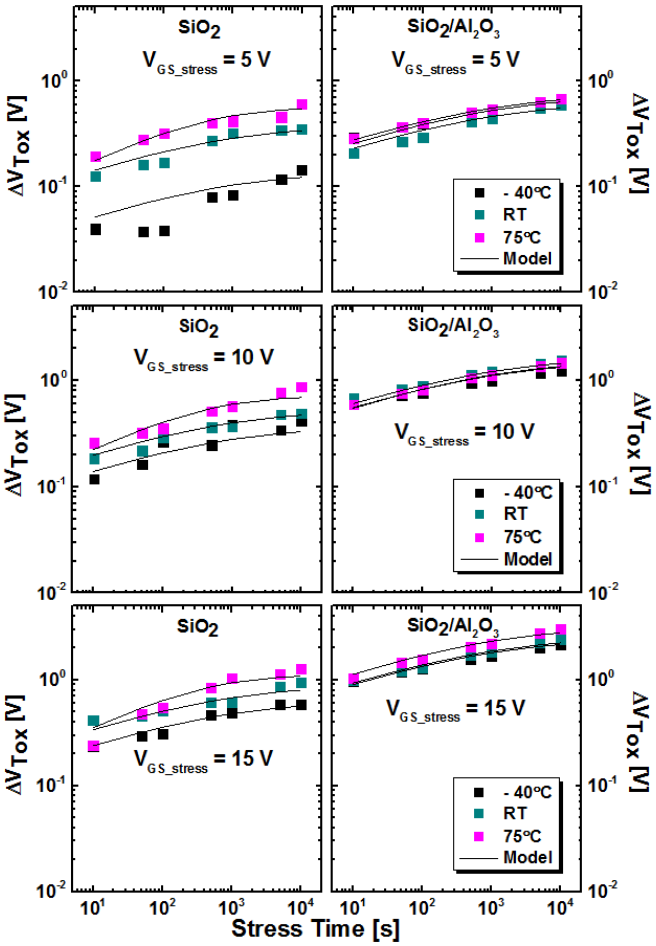

Figure 13. Model vs. experiments of ΔV_{Tox} evolution with stress time, for $V_{GS,stress}$ = 5 V, 10 V, and 15 V, at different temperature.

generation near the oxide/GaN interface. Permanent damage after harsh stress is induced in both oxide systems but of a different nature. In SiO_2 transistors, non-recoverable interface state generation takes place. In SiO_2/Al_2O_3 MOSFETs, trap states in the oxide close to the semiconductor interface appear to be created. These findings are consistent with studies on other semiconductor material systems.

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